Q5 Known Good Substrates Technical Report
CONTRACT/PR NO. N00014-07-C-0918 Dow Corning Corporation
Quarterly Technical Report
Reporting Period: 1 September 2008 – 30 November 2008

Executive Summary

Technical Progress

The following table documents the key program end metric goals.

Metric	50th Percentile	20th Percentile
MPD distribution 4H n+ 76 mm diameter (cm^{-2})	10	5
MPD distribution 4H n+ 100 mm diameter (cm^{-2})	20	10
Net scratch length by LLS relative to wafer diameter (%)	40	20
Equivalent Epitaxy Defect Density 76 mm diameter (cm^{-2})	<10	<5
Epitaxy Doping Target Accuracy	+/- 25%	+/-10%
Epitaxy Doping Variation within wafer (Max-Min/Min, %)	35%	10%
Substrate Resistivity Maximum 4H n+ 76mm	0.025	0.020

The table is now color coded to reflect the status of the program. Green=met goal; yellow=nearly met; red=not met. Details and data pertinent to the specific goals are provided in the next section of the report.

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14. ABSTRACT **The Known Good Substrates (KGS) Phase II program was initiated 29 August 2007. Wafer, epitaxy, modeling and metrology work has been the main focus of efforts in Q5. This technical report summarizes the progress by all team members against the tasks and milestones.**			
15. SUBJECT TERMS **SiC wafer, SiC epitaxy, SiC material metrology**			

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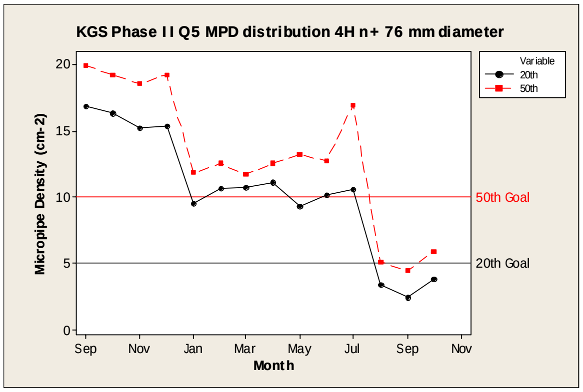
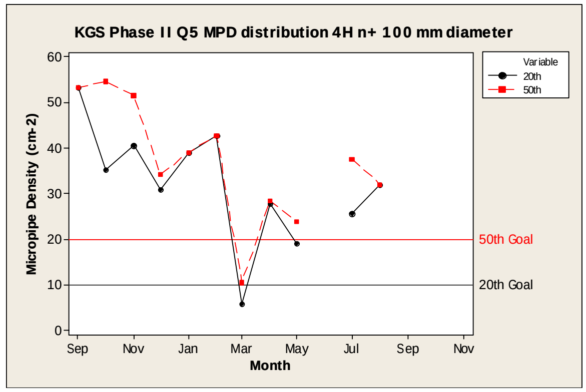
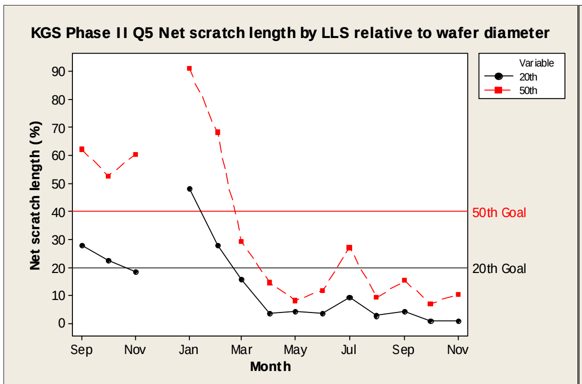
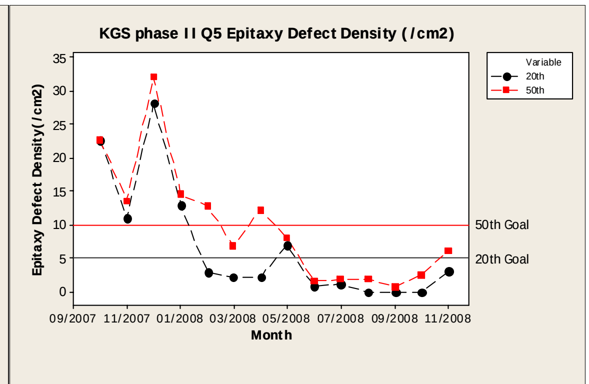
<u>Progress against Metrics</u>

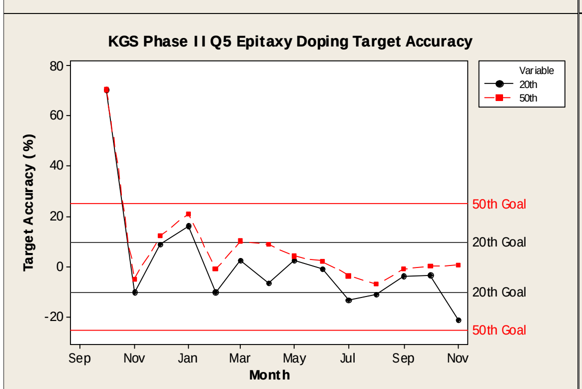
The following charts show early progress against the program metrics. Due to extended processing cycles, data tends to become available 4-6 weeks in the rears.

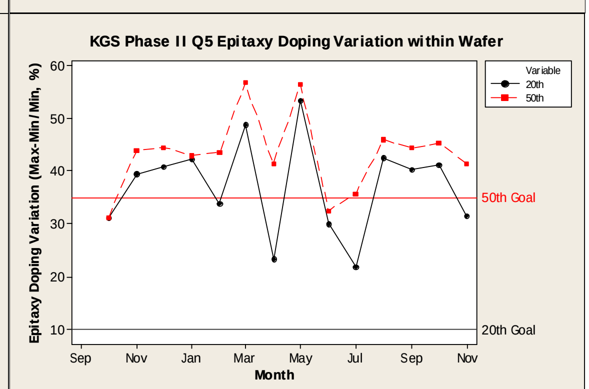


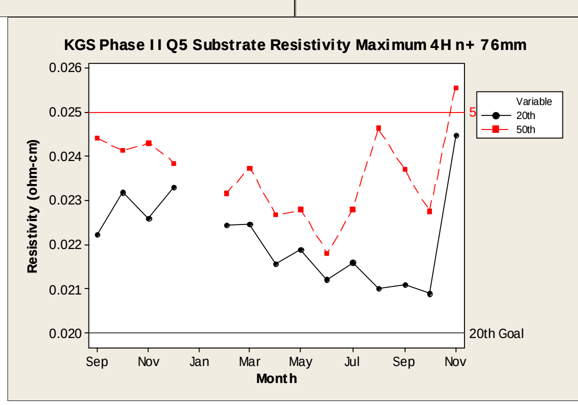












Project Milestones
Task 1: SiC Wafers Products

Highlights:

- MPD data shows a strong improvement in performance for material grown in this quarter. The 20th percentile of performance is <2 cm^{-2} while the 50th has moved to <5 cm^{-2}.
- Maximum Resistivity of material has consistently been moving towards the program targets. The 20th percentile is moving towards 0.02 Ω-cm while the 50th percentile has maintained target levels with no reduction in performance. Note: the November data is due to the low number of boules measured to date due to the long lead times between crystal growth and electrical measurements. Work in crystal growth in the late October early November focused on increasing the number of growth starts with targets to achieve maximum resistivity <0.020 ohm-cm
- Wafer polishing continues to exceed the 50th and 20th percentile goals of the program.
- Improvements in the epitaxial growth process implemented in Q3 continue to produce material with low epitaxy defect density in Q5 of the program.
- Epitaxial doping accuracy is close to target levels.

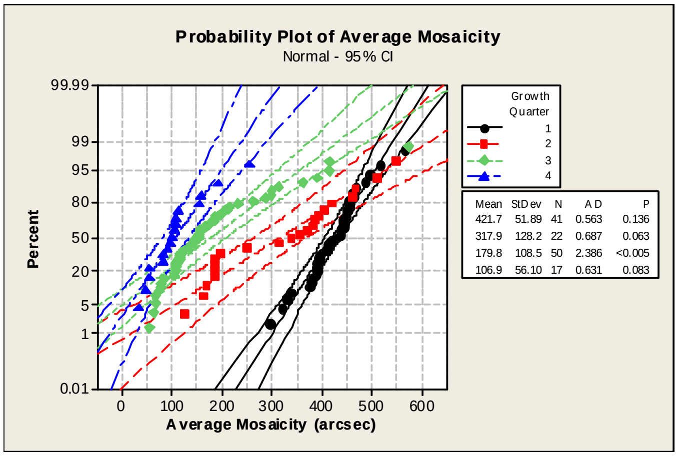
Roadblocks:

- 100 mm crystal growth is still in transition to the new PVT approach which has delivered step change improvement in 76mm crystals. MPD<20/cm2 has been demonstrated, but further adjustment of the process is still in progress. The key to the 100mm is adjustment of the thermal gradient uniformity so that the same gradient is present throughout the growth period. Currently there are issues with repeatability of the growth rate. Four 95-100 mm growths have been completed in Oct and Nov, material is being evaluated. Resistivity of 100mm materials will be addressed when the crystal growth process is stabilized. With learning obtained from the 76 mm wafer line this will be addressed in the next project phase.
- Epitaxial doping uniformity continues to be a challenge with uniformity values tracking close to the 50th percentile goal. Work to reduce the doping uniformity is driven though process modeling which has identified some promising routes to change the depletion profiles. Modifications of the reaction zone and gas system are in progress and experimental testing is expected to start in January.

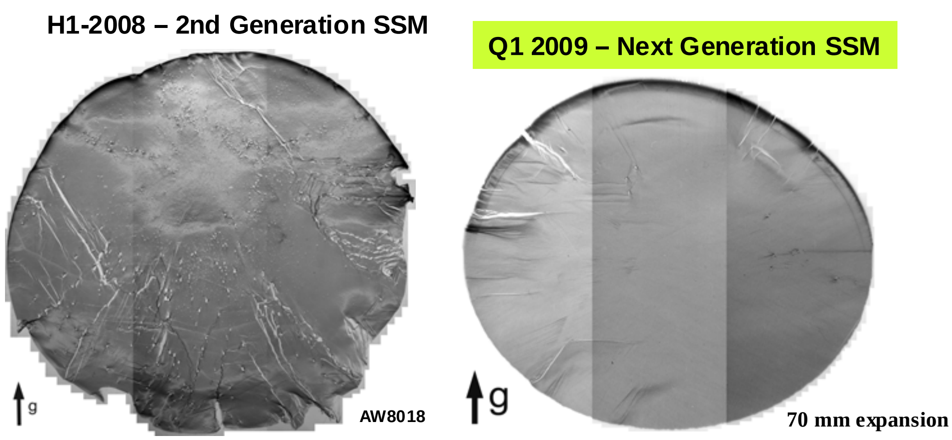
Project Milestones
Task 2: Continuous Improvements in SiC Substrates

Highlights

- Full implementation of the improved PVT growth process has resulted in material quality improvements in terms of lattice curvature and XRD full width at half maximum which have shown a 5X improvement. Current 50th percentile within wafer FWHM by rocking curve method is <100 arcsec. Year to date data is displayed below, showing steady reduction each quarter. Best competitor material is FWHM <30 arcsec. Current average within wafer omega peak variation is <0.5 degrees. Best competitor material is <0.25 degrees.



- Key project to upgrade seed stock progresses well. Expansion of small high quality crystal seeds is yielding the best 4H crystal quality measured at DCCSS ever. Example XRT data is shown below for a 76mm wafer from Q2 and a recent expansion wafer. Currently expansion is at 70mm diameter and progressing toward above 100 mm. The goal is to replace the 76mm crystal growth seed stock with improved material in Q1-2009.



- The improved growth furnace RF heat source delivered in Q3 and installed in Q4 has shown the potential to improve the crystal growth process. This will be rolled out to all production furnaces in Q6 of the program.

Roadblocks

- Key effort must focus on upgrading seed stock through expansion work.

Task 3. Metrology for wafer specifications

Highlights

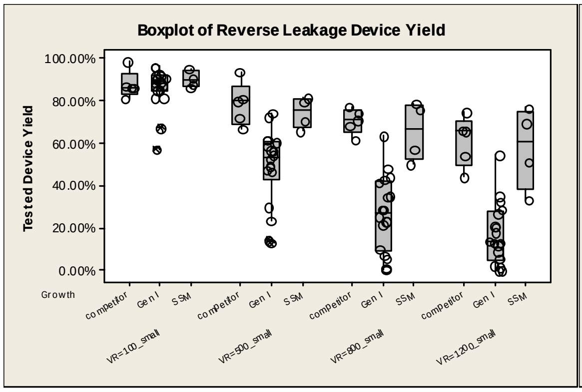
- LLS device yield prediction has been applied to JBS (Junction Barrier Schottky) diodes fabricated at MicroSemi. Delta of prediction and tested yield at low reverse bias of JBS is very comparable to that from SBD. LLS test can be used to get the full quality area test for the JBS diode application.

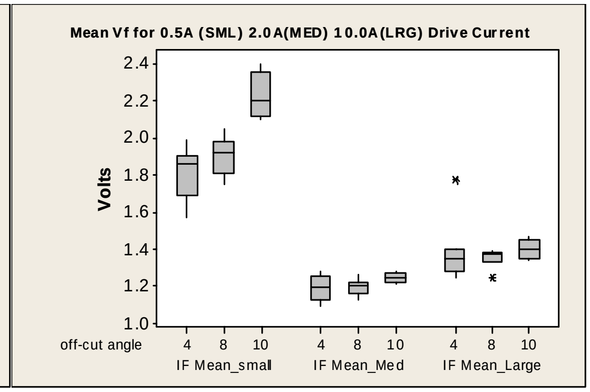
- Progress of SLIOS (Scanned laser-induced optical stress) this quarter involved imaging of *p-i-n* wafers before and after optical stressing, and developing a MATLAB program to stitch the images of adjacent areas together smoothly to produce larger area images. This technique can be successfully applied to observe stacking fault growth under optical stress in Schottky (i-n^+) wafers lacking a p^+ contact layer. The larger stitched images show correlation between substrate scratch lines and stacking faults growth in some but not all cases. Some apparently in-grown stacking faults that do not grow under stress were observed in some areas and are under further investigation. A 900 ± 100 nm filter is also attached to attempt to image dislocation related features.
- Thermal imaging of Ni/4H-SiC SBD has been carried out using both an infrared (IR) microscope (Quantum Focus Instruments Infrascope II) and nematic liquid crystal (LC) imaging. IR imaging is now in progress using black paint to eliminate emissivity variations due to surface morphological features, but hot spots we expect to observe due to low Schottky barrier height patches caused by dislocations have not yet been conclusively observed. The LC technique has also been attempted, and reproducible hot spots were observed in one case. Thermal simulations using ANSYS software were completed to understand the sensitivity issues.

Task 4. Device Technology Maturation

Highlights:

- JBS diode – 12 and 15 um epitaxial wafers have been processed to make JBS diodes at MicroSemi. Five lots and three different die sizes are employed and each lot has a competitor sourced control wafer. Both reverse and forward characteristics are evaluated on the wafer level tests. Wafers from new growth process method (SSM) shows better reverse bias leakage yield than legacy wafers and very comparable values to the competitor resourced control wafers (see figure on left, below). Small die reverse leakage data suggests some reduction of soft breakdown defects in SSM materials. Reverse leakage yield degradation rate with increasing bias of all the tested diodes is higher than DCCSS internal SBD with no edge termination. One of possible hypothesis of this is some process variation in the edge termination of JBS diode. More failure analysis is under investigation. Forward voltages (Vf) to draw specific forward current shows that DCCSS wafers have lower Vf average and smaller Vf sigma as compared to the competitor wafers (see figure on right, below- off angle “10” is competitor).





- SBD diode – five wafers have been processed to make SBDs at NRL. Four different die sizes and field plate edge termination are employed. Reverse leakage current at -100V is recorded and SBH and ideality factor are analyzed. LLS prediction matches very well with reverse leakage currents at -100V. No correlation between reverse leakage current and SBH has been observed. Surface roughness variation of 4 degree off-cut epi wafers from LLS topo image has no impact on SBH and ideality factor. Reverse leakage current @ -100V, however, shows higher values with rougher areas in the wafers. Large diode (3mm) shows lower SBH and higher ideality factor as compared to small diode (300um). This suggests some lateral SBH inhomogeneity in active diode area and needs further investigation.

Roadblocks

- Failure analysis of wafers is starting slowly. FA data expected in January. No data from NGES on SITs.

Progress toward Milestones for End of Program (Sub-bullets are progress this quarter)

• Correlation Maps of PiN forward IV characteristics and recombination lifetime
  - o Showing very good correlation between recombination lifetime and Vf of PiN

• Correlation of PiN forward IV characteristics and n+ epitaxial buffer layer/MP blocking

o PiN forward IV characteristics shows no correlation with n+ buffer layer. Carrier lifetime is a key factor to determine Vf in PiN. No significant reverse leakage current change between center and edge area of the wafers with thick n+ buffer layer and this can be attributed to micropipe dissociation with thick buffer layer.

• Primary SiC material defect limiting PiN performance (Roadmap input - GeneSiC)

-inputs to be developed in January

• SiC materials parameter assessed as most important for SIT performance
  - Improvements based on wafer probe data (Roadmap input - NGES)

-inputs to be developed in January

• SiC materials parameter assessed as most important for SBD performance improvements based on wafer probe data (Roadmap input - Microsemi)

- New process line material (SSM) shows some reduction of soft breakdown defects and good forward characteristics. Large size diode shows more SBH inhomogeneity.

• Generational improvement of 4H SiC wafer crystal quality summarized by XRT and MPD analysis

- X-ray topographs were carried out on recent SSM growths. The resulting topographs show a continued improvement of the crystal quality.

• Assessment of oxide quality for 76mm/100mm 4H epiwafers and link to generation lifetime

- Generation lifetimes are very sensitive to process conditions prior to oxidation and oxidizing process. Need metrics to better assess the quality and reproducibility of the oxide.

Appendix 1: KGS Subcontractors and Quarterly Progress Points

Subcontractor	Area of Focus	Progress This Quarter
Northrup Grumman Electronics Systems	J-SIT fabrication and testing	Still waiting for device results.
Microsemi	SBD fabrication and testing	SBD are fabricated and tested. Wafer level testing data are analyzed. DCCSS wafers show good forward characteristics. High yield degradation rate with increasing bias is observed. More FA is underway.
GeneSiC Semiconductors	PiN diode fabrication and testing	Final report in progress. Record forward and reverse performance demonstrated.
SUNY – Stoney Brook	Crystal Structure of SiC	XRT testing shows continuous improvement of the crystal quality with SSM materials
Arizona State University	SiC Oxides, carrier lifetime and device failure analysis	Stitched PL images show better correlation between SF and substrate scratch lines.
Fluxtrol	Modeling and design of high uniformity induction heating systems	Project completed, new heaters have demonstrated better crystal quality and process consistency.
NRL	SiC Oxides, Epitaxy, Lifetime testing, materials testing, device testing	SBD diode are fabricated and tested. Large diodes show more SBH

		inhomogeneity. PiN fabrication is started.
STR	Modeling of CVD and PVT SiC Growth Processes	Modeling of CVD Epitaxy processes has provided key insights to understanding the sources of doping variations observed in the batch epitaxy reactor.